IN THE CLAIMS

Please amend claim 37 as set forth below.

1. - 36. (Canceled)

37. (Currently Amended) A semiconductor memory apparatus comprising:

a plurality of semiconductor memory devices;

each of said semiconductor memory devices comprising a source region and a drain region, a semiconductor current path connected between the source and the drain regions, a plurality of small charge storage nodes surrounded by an insulator which acts as a potential barrier for the charge storage nodes, wherein said charge storage node is located between ~~said~~a control electrode ~~gate~~ and said current path;

wherein said plurality of semiconductor memory devices stores information by a difference of an electron charge stored in each said charge storage node;

a plurality of said control electrodes ~~gates~~ connected to each other between a plurality of said semiconductor memory devices; ~~and~~

wherein a voltage applied between the source and the drain region in the semiconductor memory device is different

according to the difference in information to be written in a writing operation for different information stored in each of said plurality of semiconductor memory device which is driven by a same word line; and

wherein a threshold voltage varies within a relatively small range when a relatively small voltage is applied between said source and drain regions, and a threshold voltage varies within a relatively large range when a relatively large voltage is applied between said source and drain regions.

38. - 40. (Withdrawn)

41. (Previously Amended) The semiconductor memory device according to claim 37, wherein the source and drain regions and the current path is located on an insulator film.